FIG. 1 (CONVENTIONAL ART)

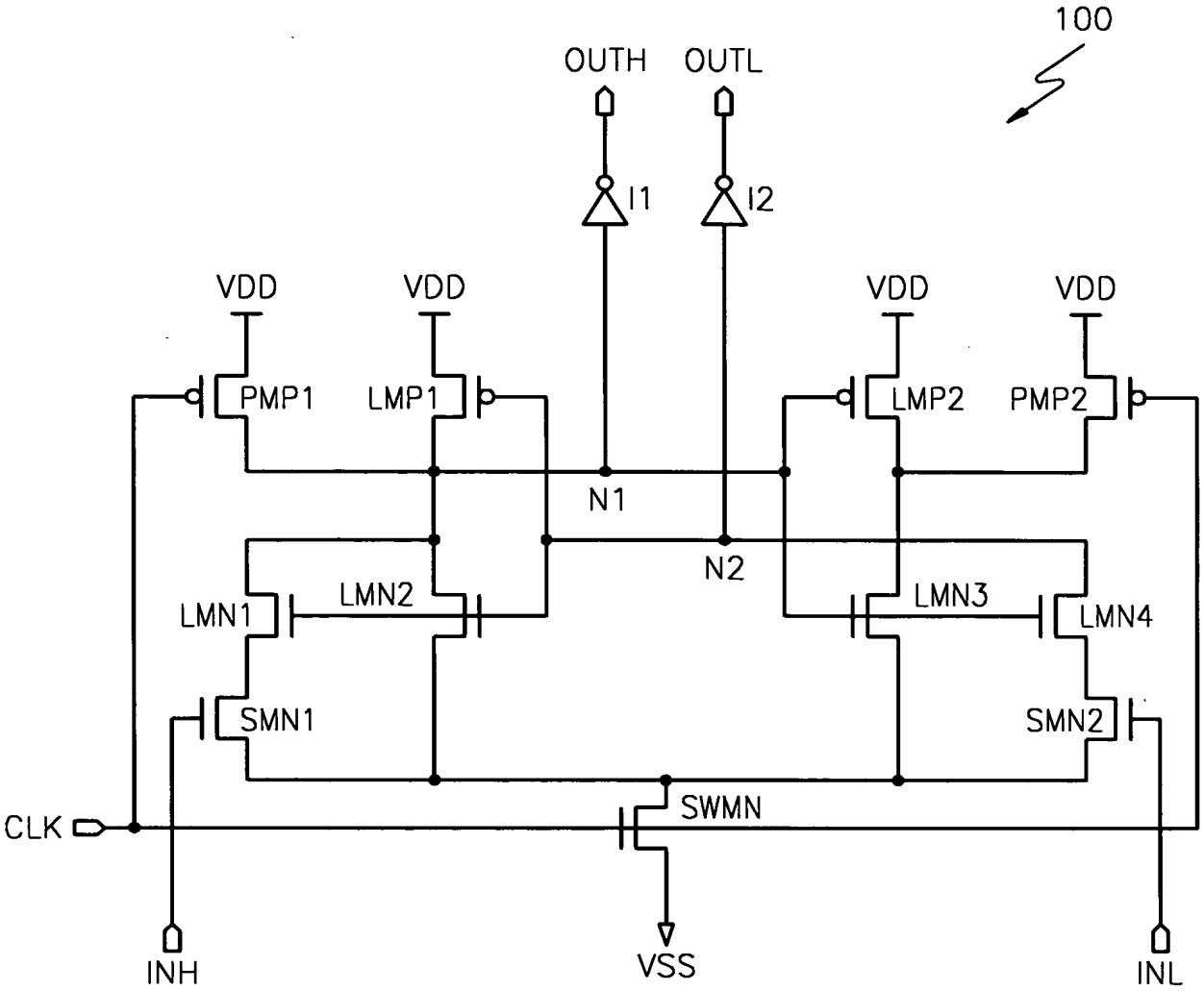
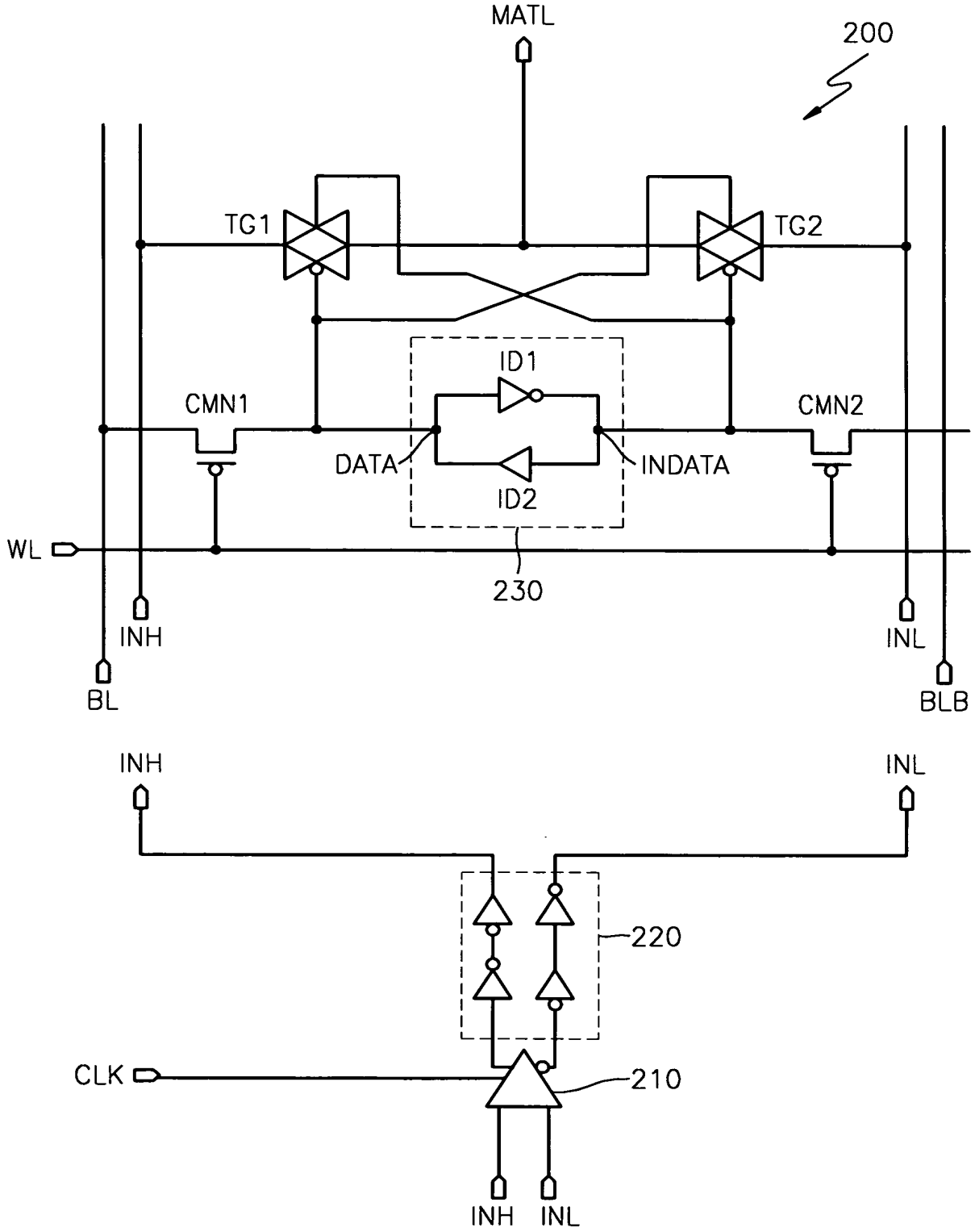


FIG. 2 (CONVENTIONAL ART)



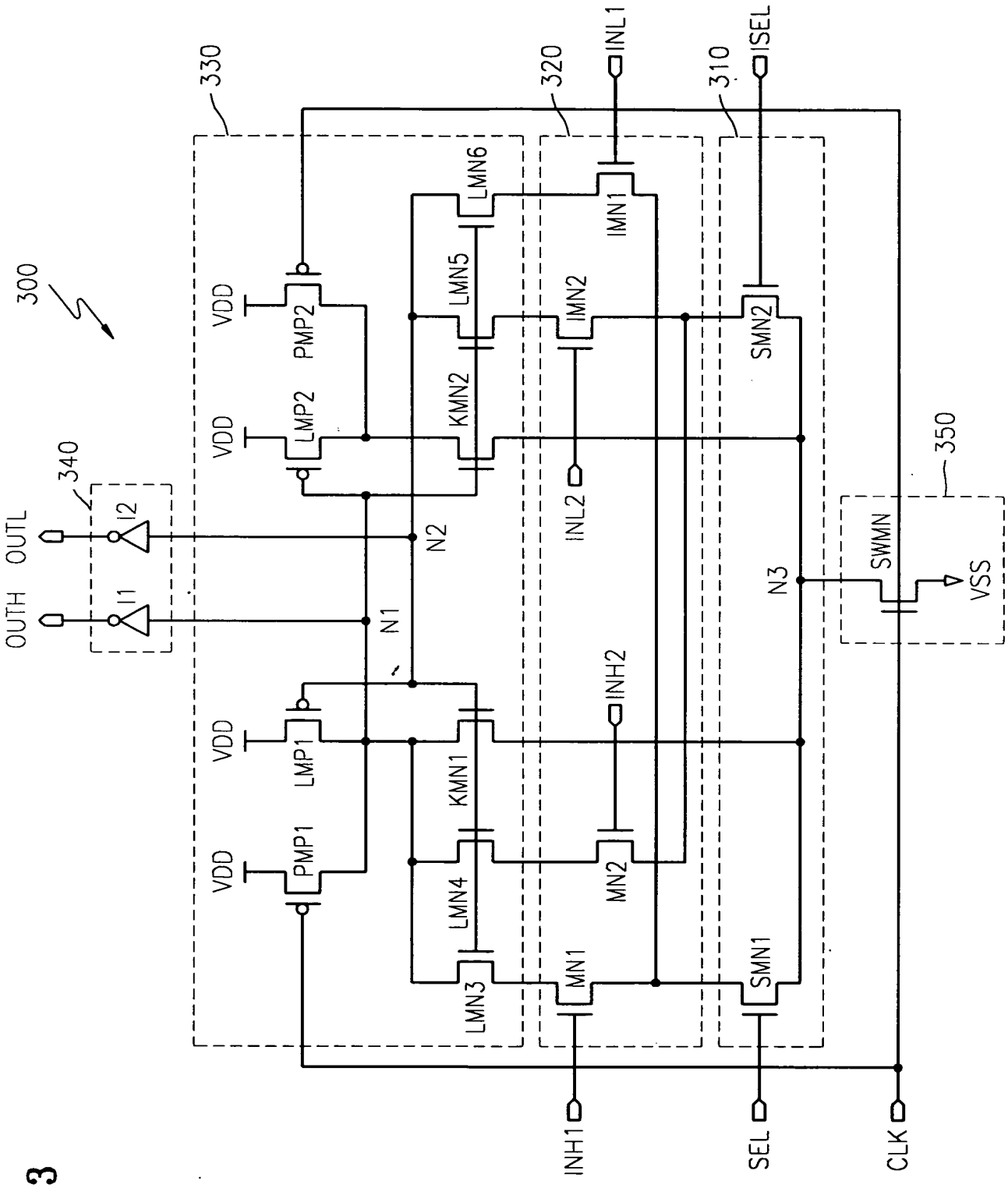

300
330
320
310
INL1
ISEL
IMN1
LMN6
LMN5
IMN2
SMN2
VDD
PMP2
LMP2
KMN2
340
I2
I1
OUTH
OUTL
N2
N1
INL2
N3
350
SWMN
VSS
INH2
LMP1
KMN1
PMP1
LMN4
MN2
LMN3
MN1
SMN1
INH1
SEL
CLK

FIG. 3

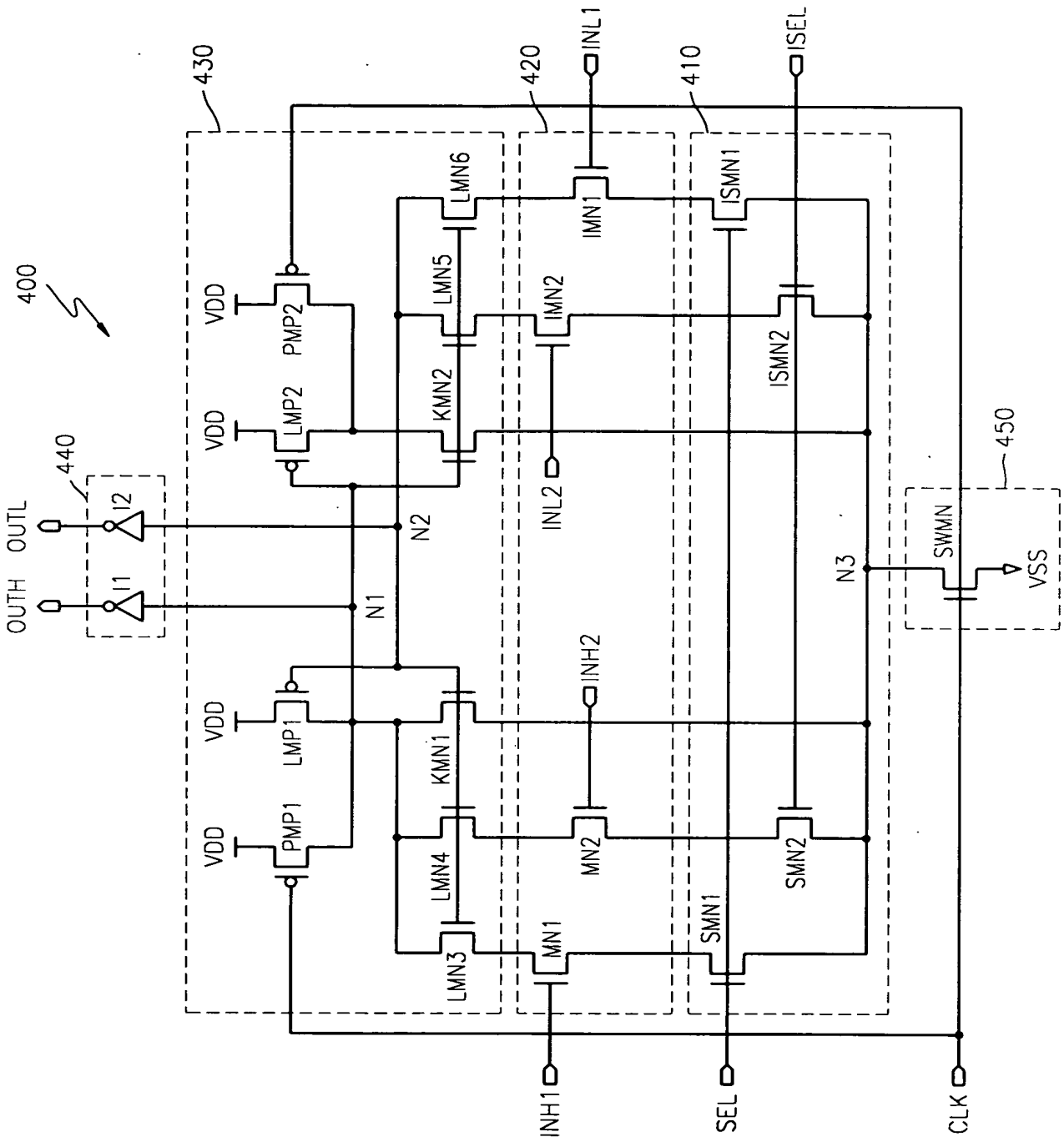

400
430
420
410
INL1
ISEL
LMN6
IMN1
ISMN1
LMN5
IMN2
ISMN2
KMN2
VDD
PMP2
LMP2
440
OUTH
OUTL
I2
I1
N2
N1
INL2
N3
450
SWMN
VSS
INH2
LMP1
KMN1
PMP1
LMN4
MN2
SMN2
LMN3
MN1
SMN1
INH1
SEL
CLK

FIG. 4

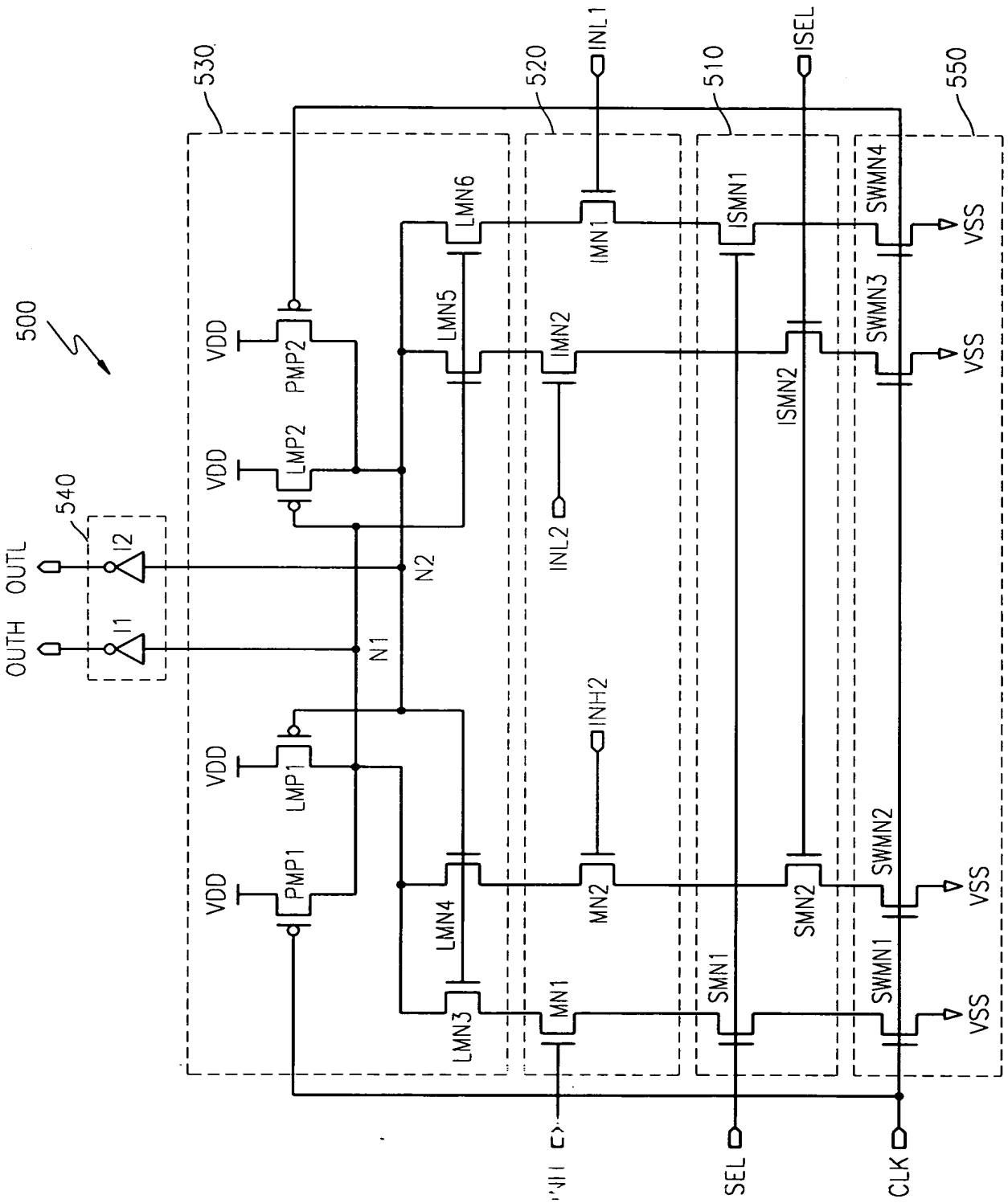

500
530
520
510
550
540
OUTH
OUTL
I1
I2
N1
N2
VDD
PMP1
PMP2
LMP1
LMP2
LMN3
LMN4
LMN5
LMN6
MN1
MN2
IMN1
IMN2
SMN1
SMN2
ISMN1
ISMN2
SWMN1
SWMN2
SWMN3
SWMN4
VSS
INL1
INL2
INH2
ISEL
SEL
CLK

FIG. 5

FIG. 6

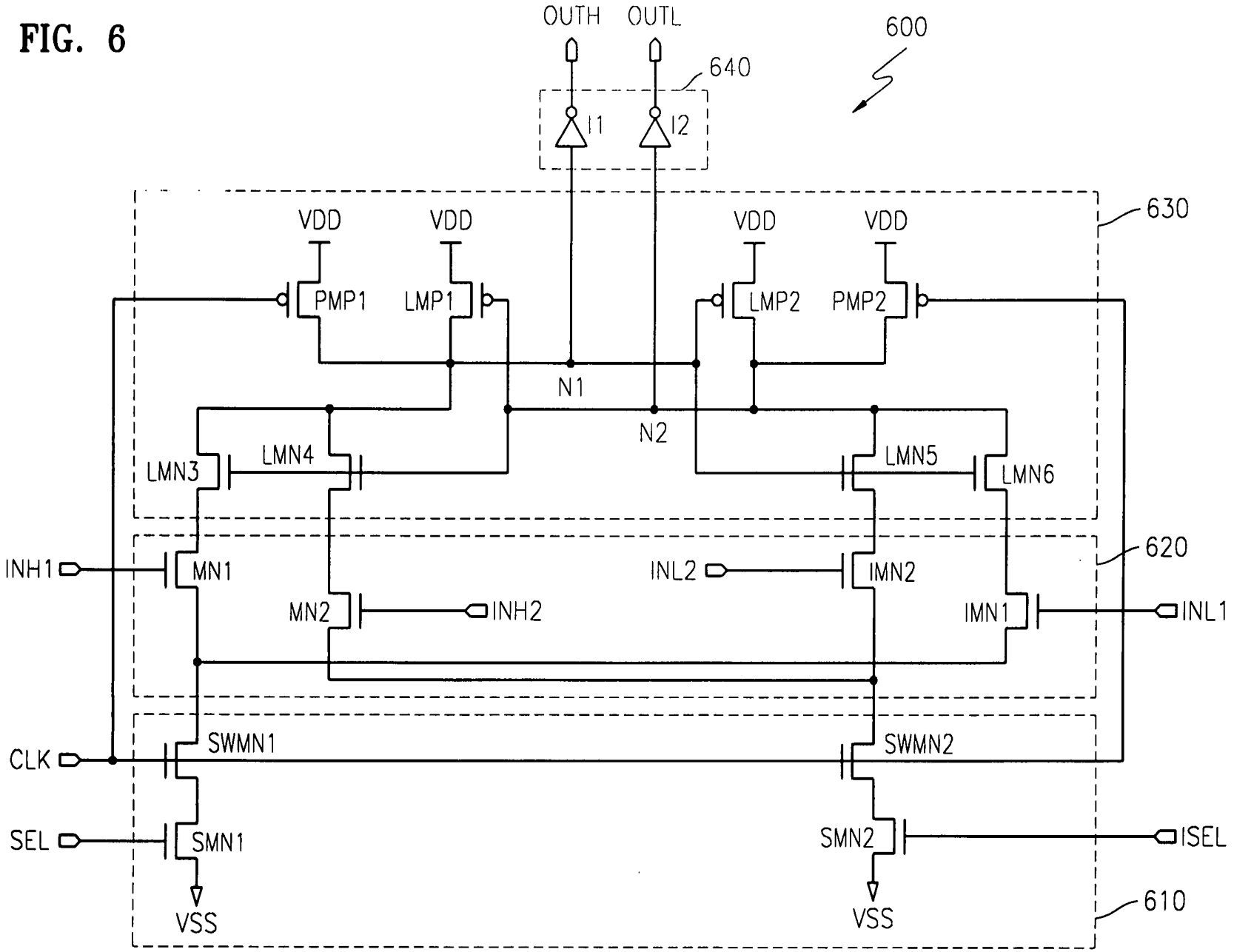

OUTH
OUTL
600
640
I1
I2
630
VDD
VDD
VDD
VDD
PMP1
LMP1
LMP2
PMP2
N1
N2
LMN3
LMN4
LMN5
LMN6
620
INH1
MN1
INL2
IMN2
MN2
INH2
IMN1
INL1
CLK
SWMN1
SWMN2
SEL
SMN1
SMN2
ISEL
VSS
VSS
610

FIG. 7

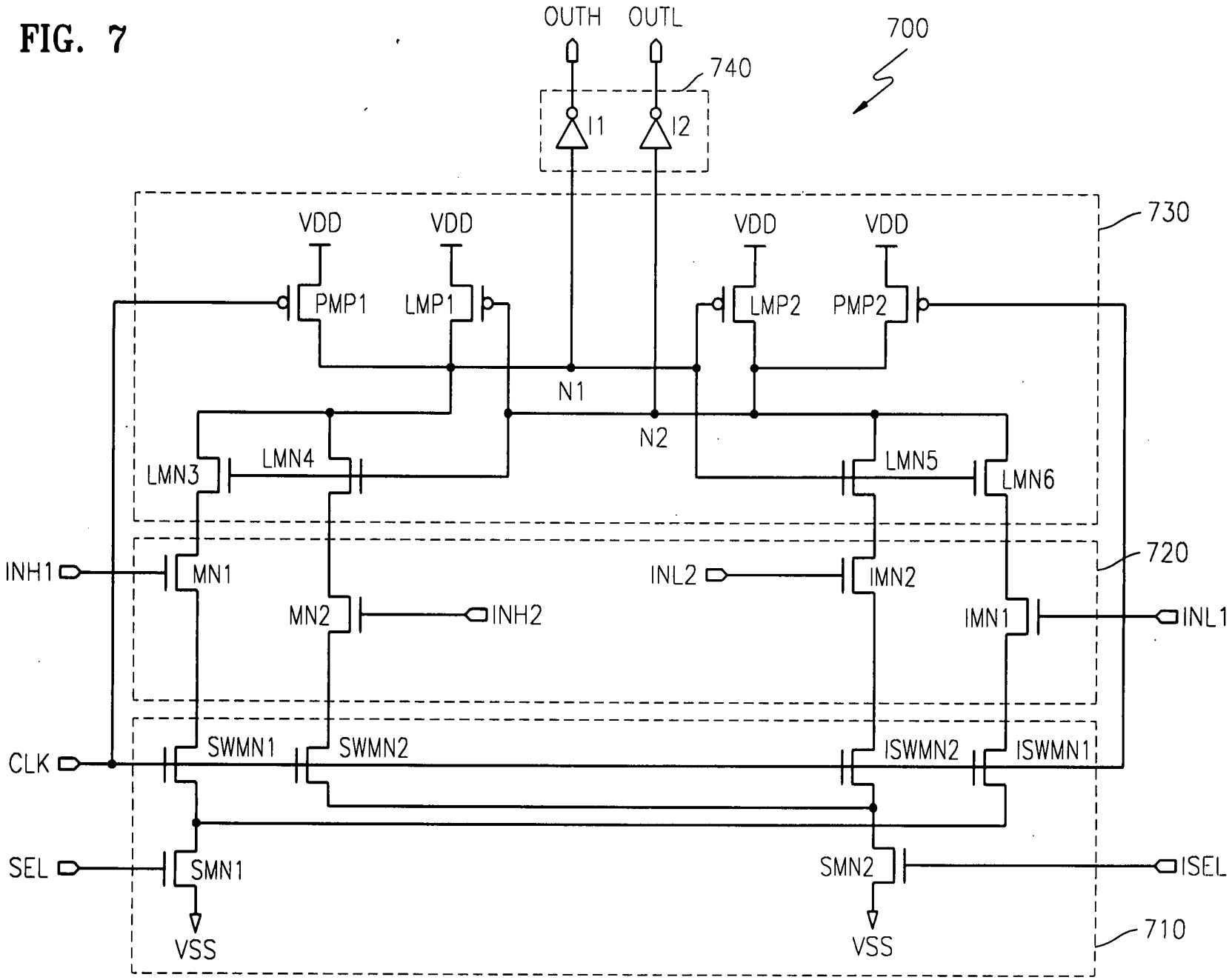
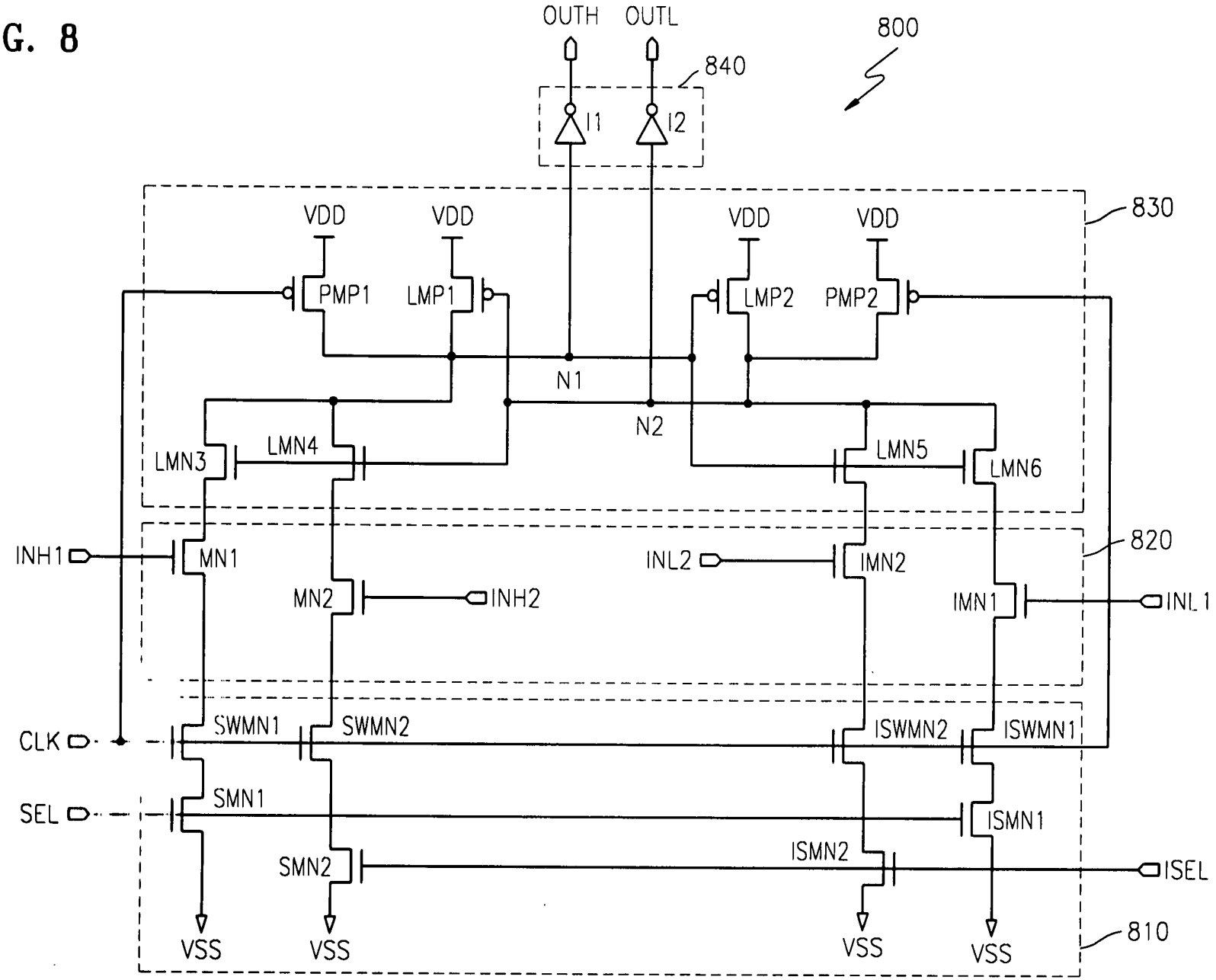

OUTH
OUTL
700
740
I1
I2
730
VDD
VDD
VDD
VDD
PMP1
LMP1
LMP2
PMP2
N1
N2
LMN3
LMN4
LMN5
LMN6
720
INH1
MN1
INL2
IMN2
MN2
INH2
IMN1
INL1
CLK
SWMN1
SWMN2
ISWMN2
ISWMN1
SEL
SMN1
SMN2
ISEL
VSS
VSS
710

FIG. 8


OUTH
OUTL
800
840
I1
I2
830
VDD
VDD
VDD
VDD
PMP1
LMP1
LMP2
PMP2
N1
N2
LMN3
LMN4
LMN5
LMN6
820
INH1
MN1
INL2
IMN2
MN2
INH2
IMN1
INL1
CLK
SWMN1
SWMN2
ISWMN2
ISWMN1
SEL
SMN1
ISMN1
ISMN2
SMN2
ISEL
VSS
VSS
VSS
VSS
810

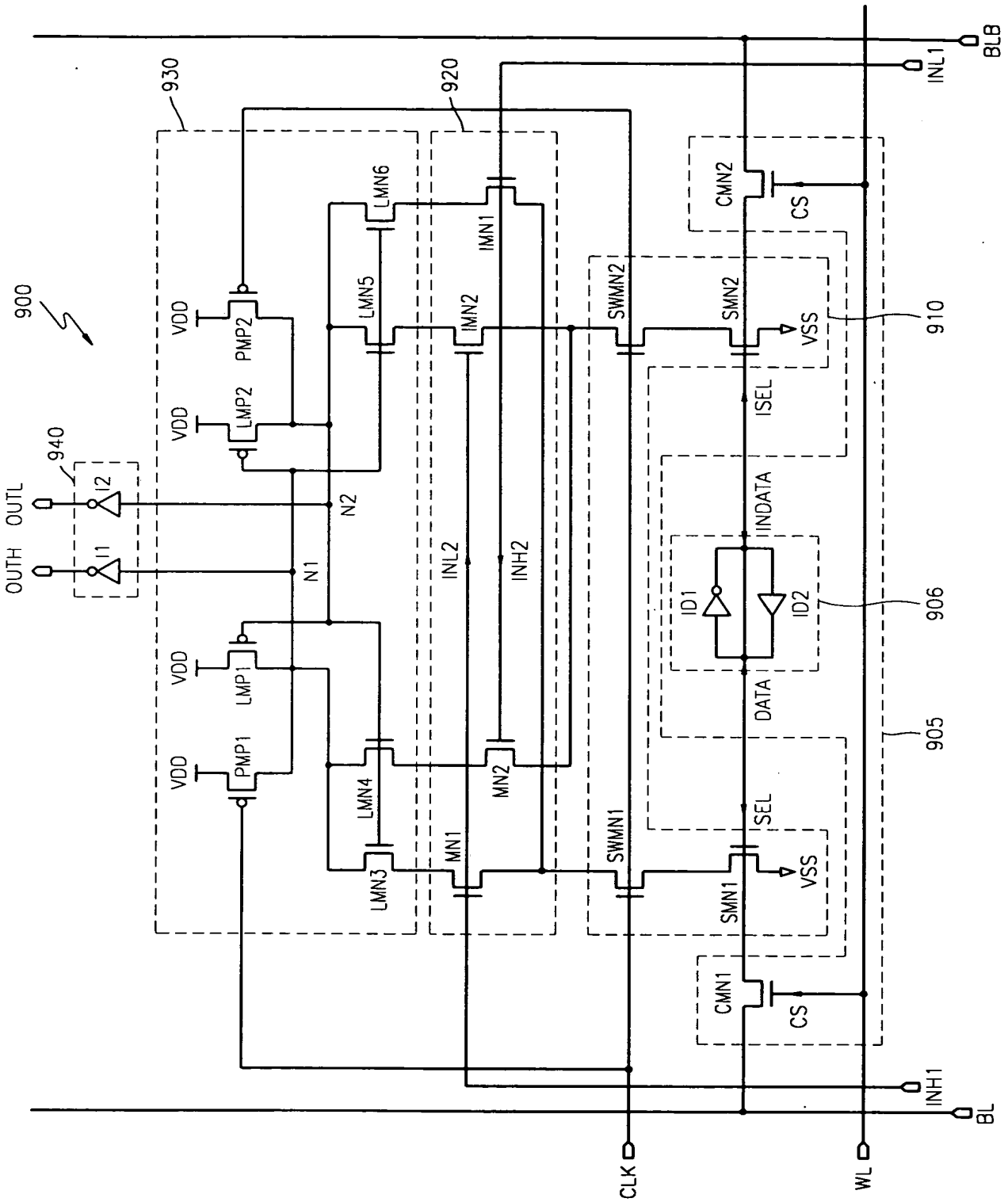

900
930
920
910
906
905
940
OUTH
OUTL
I1
I2
N1
N2
VDD
PMP1
PMP2
LMP1
LMP2
LMN1
LMN2
LMN3
LMN4
LMN5
LMN6
MN1
MN2
INL2
INH2
IMN1
IMN2
SWMN1
SWMN2
SMN1
SMN2
VSS
SEL
ISEL
DATA
INDATA
ID1
ID2
CMN1
CMN2
CS
CLK
WL
BL
BLB
INH1
INL1

FIG. 9

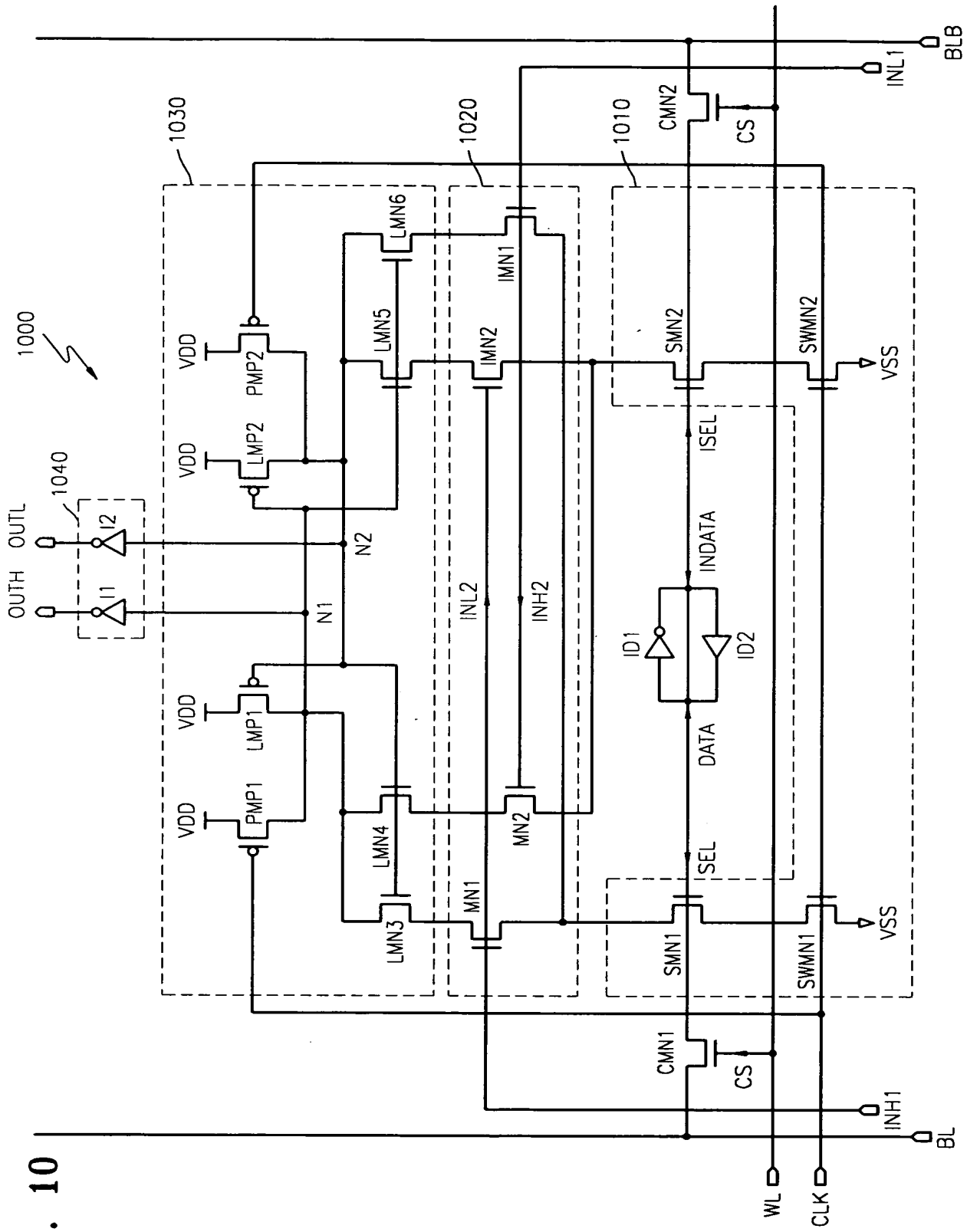
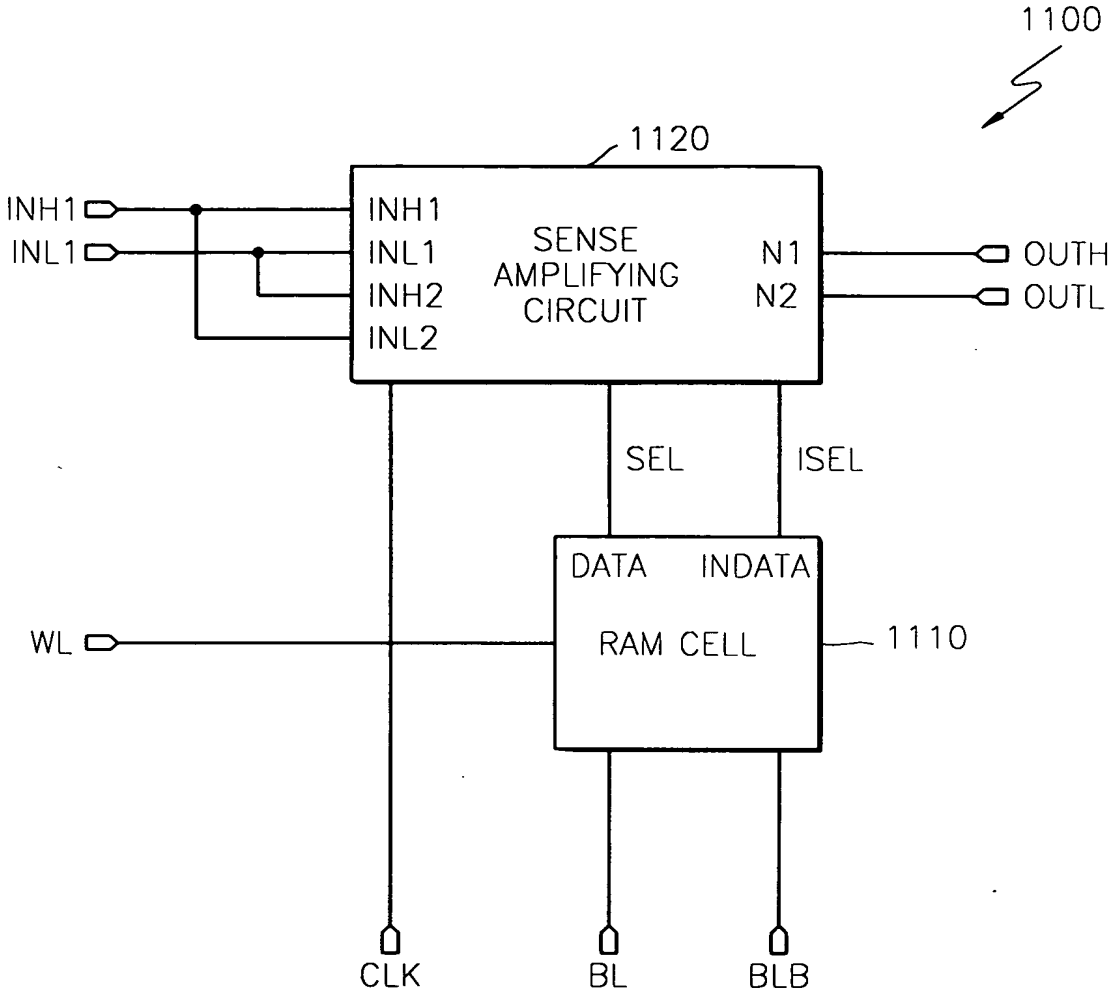

1000
1010
1020
1030
1040
BLB
INL1
CMN2
CS
VDD
PMP2
LMP2
LMN6
LMN5
IMN1
IMN2
SMN2
SWMN2
VSS
ISEL
INDATA
OUTH
OUTL
I2
I1
N1
N2
INL2
INH2
ID1
ID2
LMP1
PMP1
LMN4
LMN3
MN1
MN2
DATA
SEL
SMN1
SWMN1
CMN1
INH1
BL
WL
CLK

FIG. 10

FIG. 11


1100
1120
INH1
INL1
INH1
INL1
INH2
INL2
SENSE AMPLIFYING CIRCUIT
N1
N2
OUTH
OUTL
SEL
ISEL
DATA
INDATA
RAM CELL
1110
WL
CLK
BL
BLB